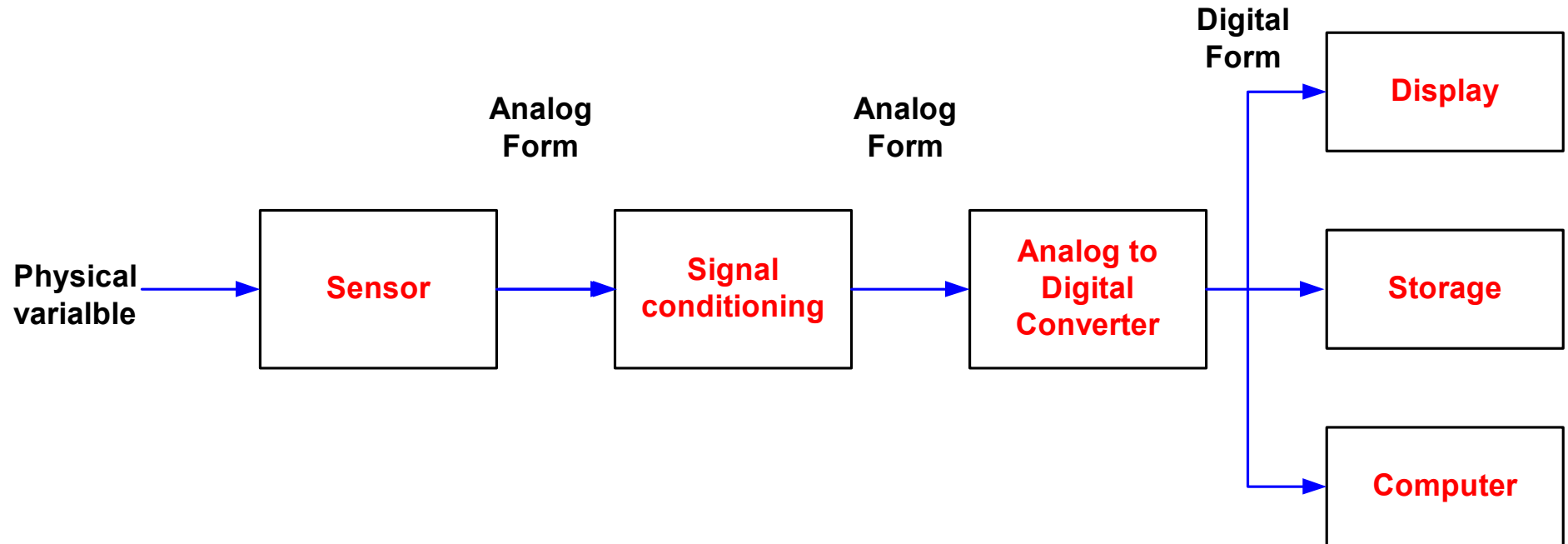


2141-375

Measurement and Instrumentation

**Sampling, Digital Devices, and
Data Acquisition**

Basic Data Acquisition System



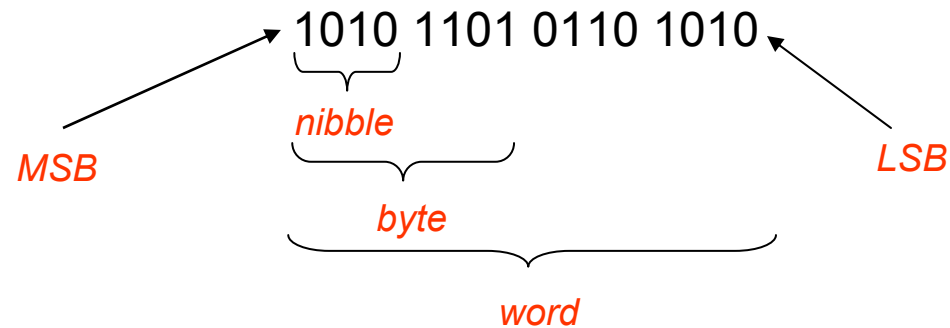
Advantages of Data Acquisition System

Efficient in managing a large amount of data
Rapid and intelligent data processing using digital computer

Numbering System: Binary Code

The digital signals are formed by only two voltage values HI and LOW, or level 1 and level 0 and it is called binary digital signal. Therefore, the information contained in the digital signal is represented by the combination of the numbers 1 and 0.

Binary numbers are comprised of the digits 0 and 1 and are based on powers of 2. Each digit of a binary number, 0 or 1, is called a bit. Four bits together is a nibble, 8 bits is called a byte. (8, 16, 32, 64 bit arrangements are also called words)



The left most bit is called the Least Significant Bit (LSB)
The right most bit is called the Most Significant Bit (MSB).

Numbering Conversion

Binary to Decimal Conversion

The conversion of a binary number to a decimal number may be accomplished by taking the successive powers of 2 and summing for the result.

$$\begin{array}{ccccccc} & 0 & & 1 & & 0 & & 1 \\ & \downarrow & & \downarrow & & \downarrow & & \downarrow \\ & 0 \times 2^3 & + & 1 \times 2^2 & + & 0 \times 2^1 & + & 1 \times 2^0 \\ \underbrace{\hspace{1.5cm}} & & & \underbrace{\hspace{1.5cm}} & & \underbrace{\hspace{1.5cm}} & & \underbrace{\hspace{1.5cm}} \\ & 0 & + & 4 & + & 0 & + & 1 & = & 5_{10} \end{array}$$

Numbering Conversion

Decimal to Binary Conversion

The conversion of a decimal number to a binary number is accomplished by successively dividing the decimal number by 2 and recording the remainder as 0 or 1

			Remainder	
$\frac{62}{2}$	=	31	+	0
$\frac{31}{2}$	=	15	+	1
$\frac{15}{2}$	=	7	+	1
$\frac{7}{2}$	=	3	+	1
$\frac{3}{2}$	=	1	+	1
$\frac{1}{2}$	=	0	+	1

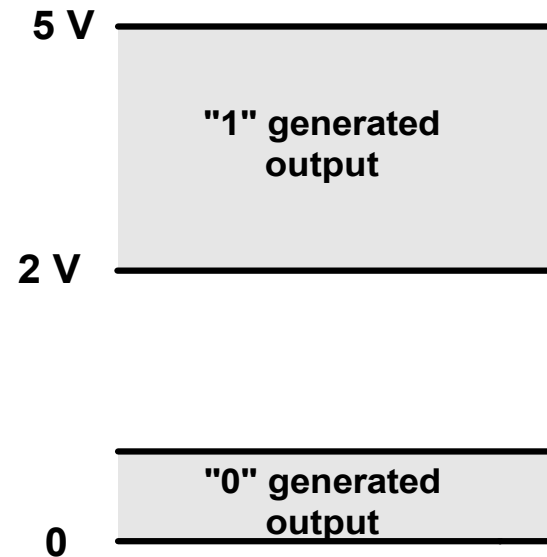
LSB

0011 1110₂

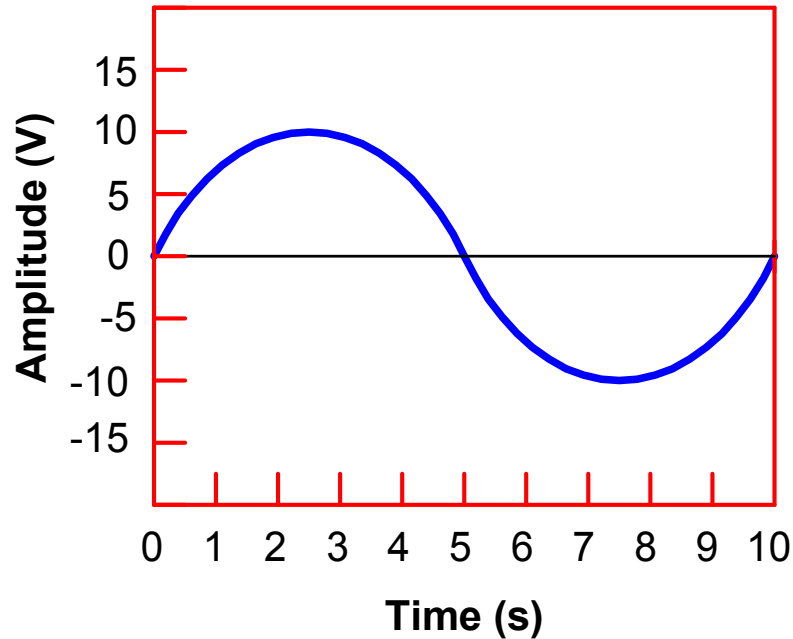
MSB

Logic Level

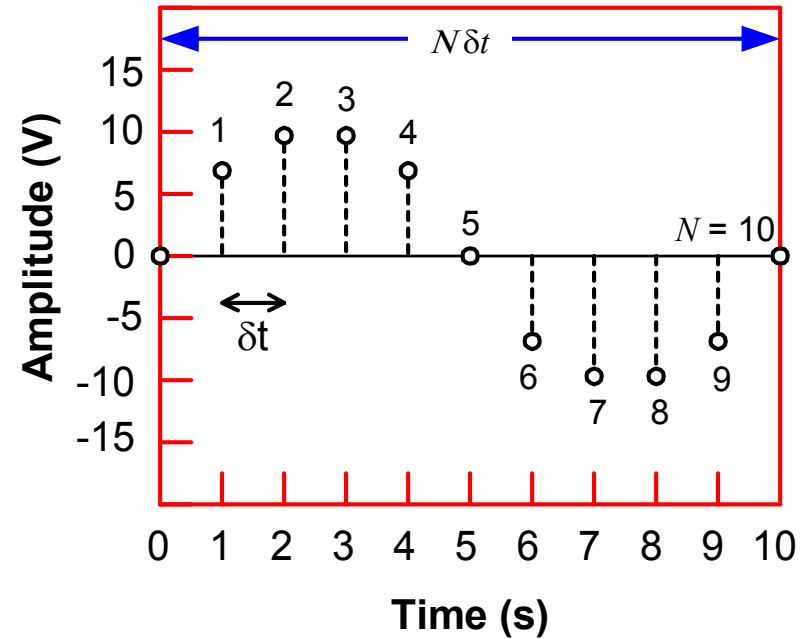
In most digital systems, the state 1 corresponds to a voltage range from 2 V to 5 V while the state 0 corresponds to a voltage range from a fraction of a volt to 1 volts.



Sampling Concepts



Analog signal



Discrete time signal

Sampling is a process that generate a discrete time or digital signal from a continuous time signal

The fundamental question therefore is how to sample a continuous time signal so that the resulting sampled signal retains the information of the original signal.

Discrete Fourier Transform

Discrete Fourier Transform (DFT) of y_r

$$y_r = y(r\delta t) \quad r = 1, 2, \dots, N$$

$$Y(f_k) = \frac{2}{N} \sum_{r=1}^N y(r\delta t) e^{-i2\pi rk/N} \quad k = 1, 2, \dots, \frac{N}{2}$$

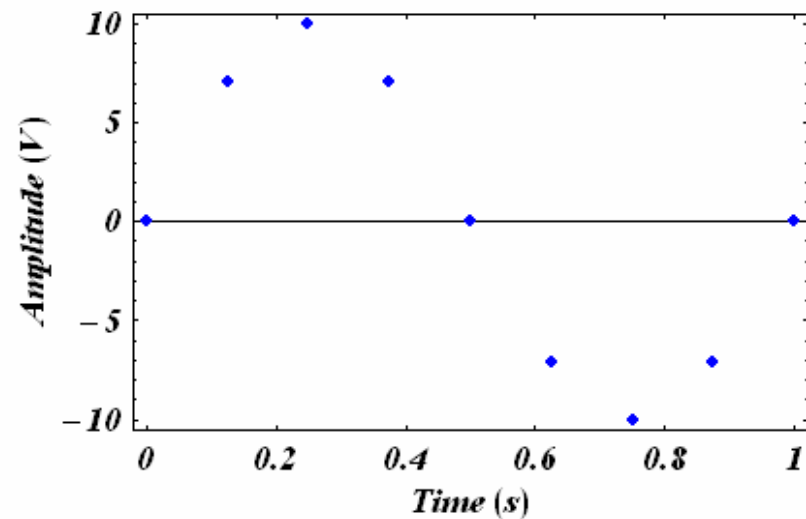
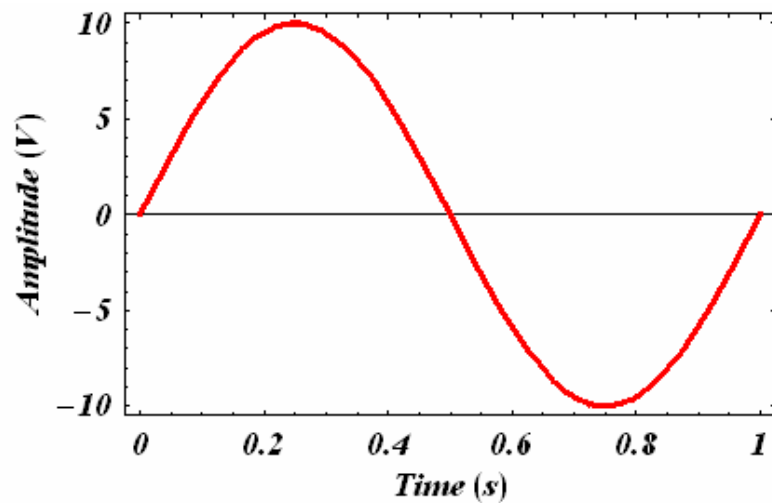
where $f_k = k\delta f$ and $\delta f = \frac{1}{N\delta t} = \frac{f_s}{N}$

Discrete Fourier Transform

Example: Estimate the amplitude spectrum or frequency content of the discrete data taken from $y(t) = 10 \sin 2\pi t$ using a time increment of 0.125 s for the duration of 1 s.

Known: $\delta t = 0.125$ s or $f_s = 8$ Hz

Solution:



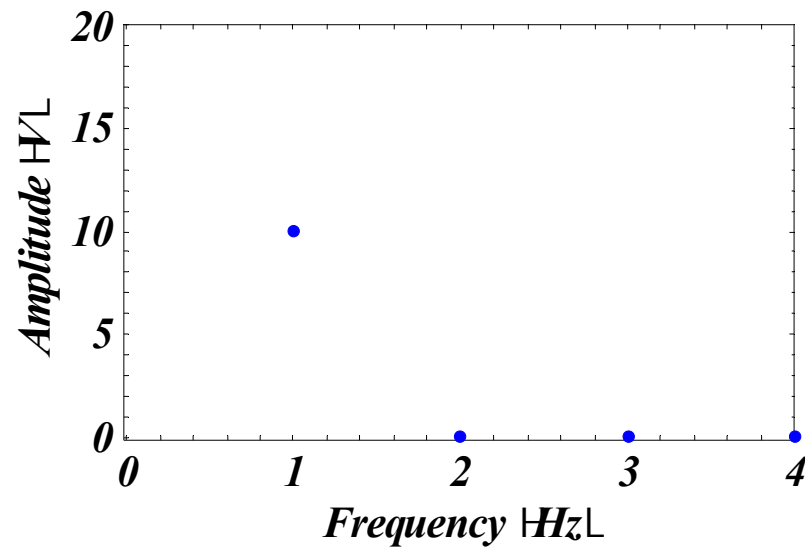
Discrete Fourier Transform

Discrete Data Set for $y(t) = 10 \sin 2\pi t$

r	$y(r \delta t)$
1	7.071
2	10.000
3	7.071
4	0.000
5	-7.071
6	-10.000
7	-7.071
8	0.000

Discrete Fourier Transform of $y(t)$

k	f_k (Hz)	$Y(f_k)$	$ Y(f_k) $
1	1	-10i	10
2	2	0	0
3	3	0	0
4	4	0	0



Sample Rate

In order to be able to reconstruct the original signal from the sampled signal the following two related constraints must be satisfied.

1. The original signal must be band-limited (i.e. must have a finite frequency content)

2. The samples must be taken with a sampling frequency which is higher than twice the highest frequency present in the original signal. (Sampling Theorem or the Nyquist-Shannon Sampling Theorem)

Sampling rate: $f_s = 1 / \delta t$

The sampling rate requires $f_s \geq 2f_m$

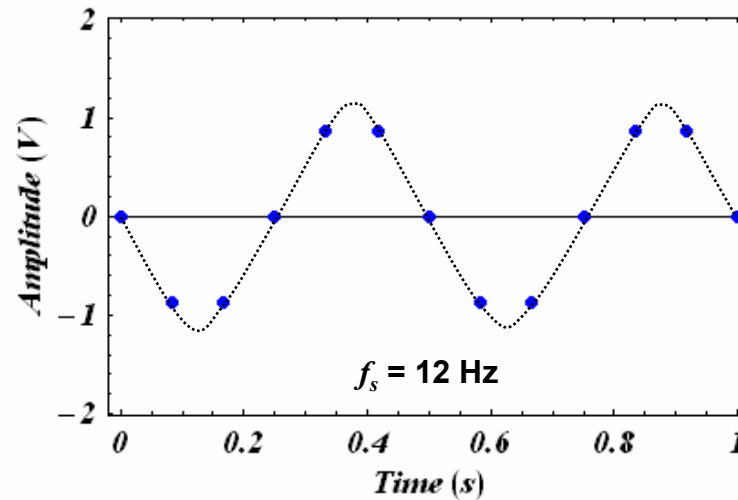
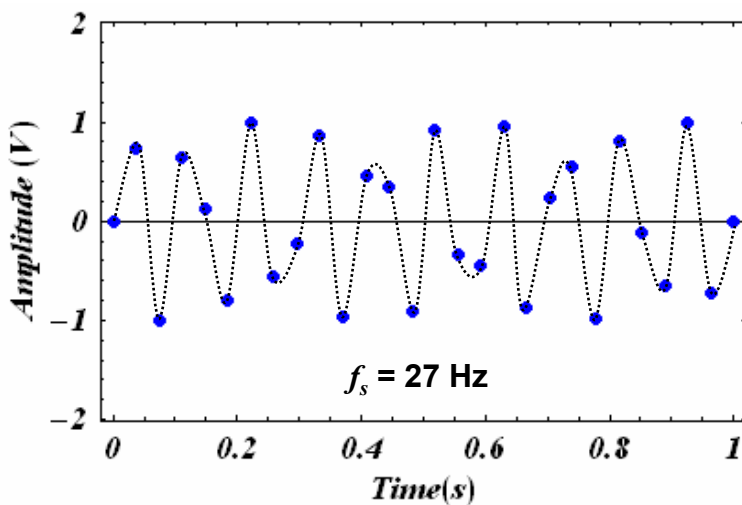
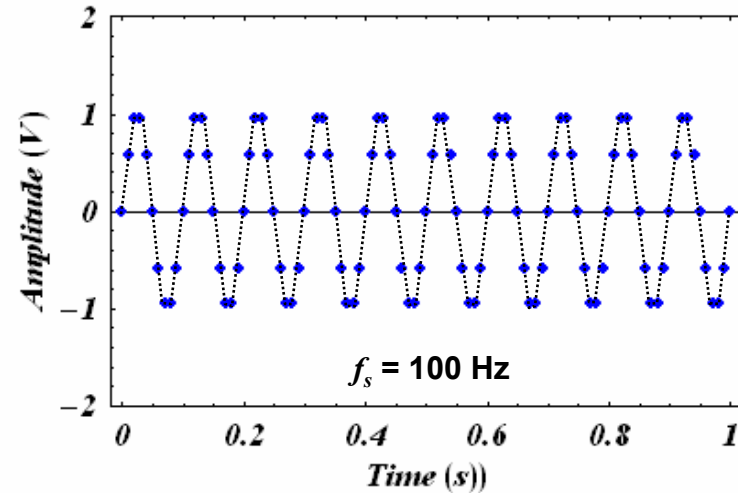
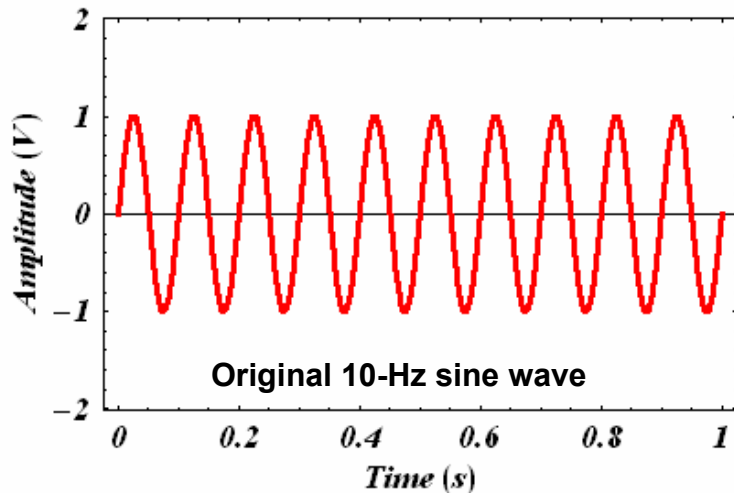
where f_m is the maximum frequency in the analog signal

Or in terms of the sample time increment

$$\delta t \leq \frac{1}{2f_m}$$

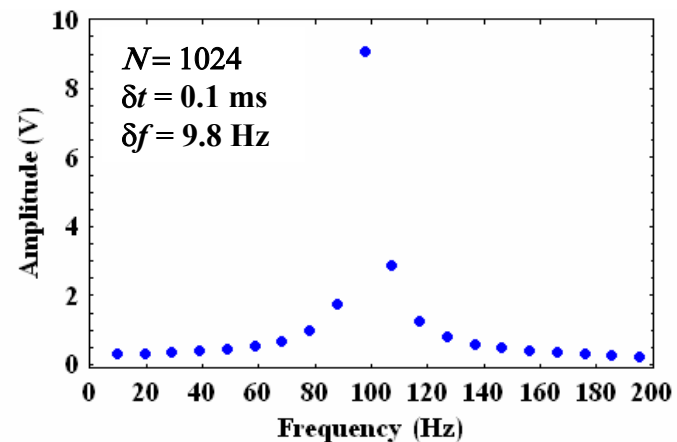
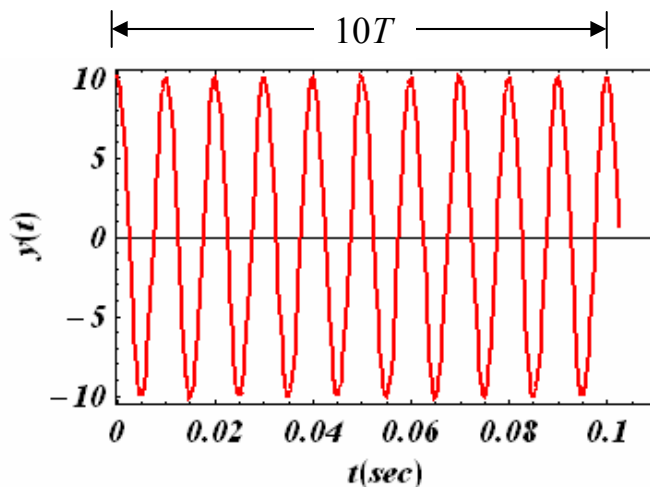
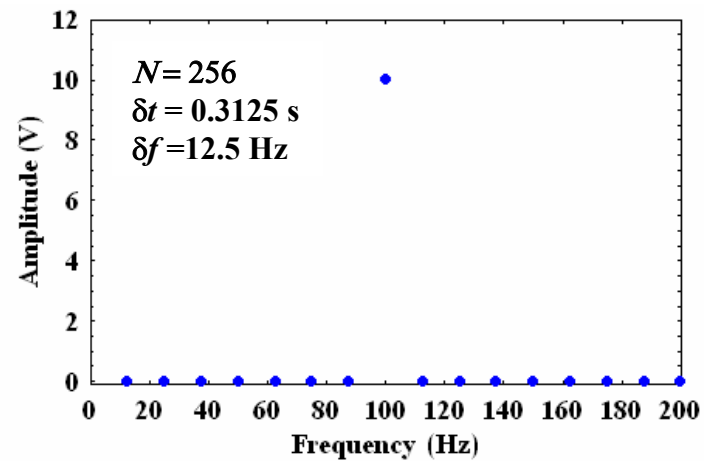
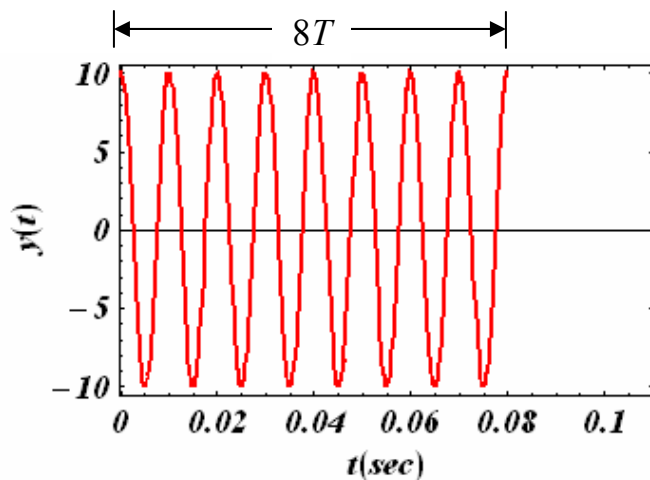
Sample Rate: Alias Frequency

When the sampling frequency is less than twice the bandwidth of a signal the time continues signal can not reconstructed from the samples.



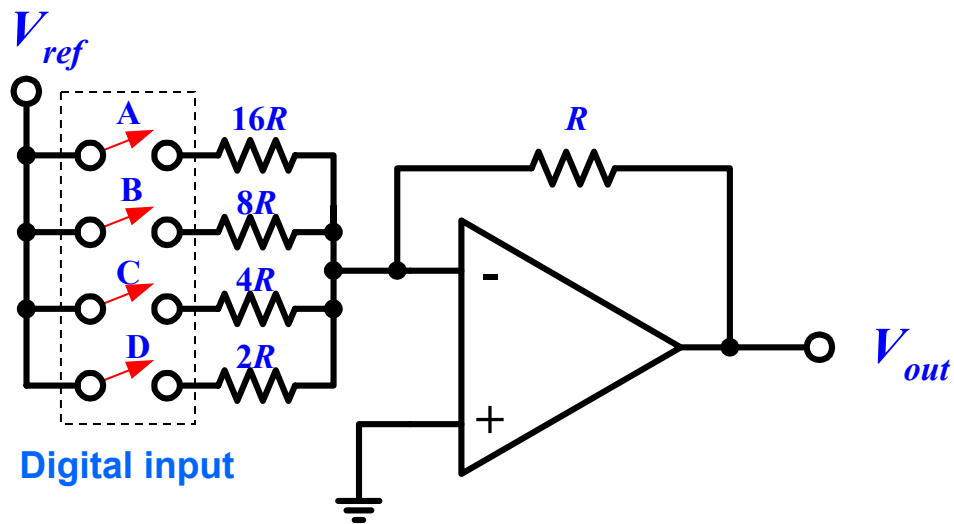
Amplitude Ambiguity

Another problem appears when $N\delta t$ is not coincident with an integer multiple of the fundamental period of $y(t)$. The problem occurs by the truncation of a complete cycle of the signal.



Digital to Analog Conversion (D/A)

The digital to analog converter (D/A) is an M-bit digital device that converts a digital binary word into an analog voltage.



In case of $A = 1$ and B, C and $D = 0$, $V_o = V_i / 16$
 $B = 1$ and A, C and $D = 0$, $V_o = V_i / 8$
 $C = 1$ and A, B and $D = 0$, $V_o = V_i / 4$
 $D = 1$ and A, B and $C = 0$, $V_o = V_i / 2$

Here $V_i = V_{ref}$

An example of D/A converter

Digital to Analog Conversion (D/A)

Digital inputs <i>D C B A</i>	Analog output
0 0 0 0	0
0 0 0 1	$V_i/16$
0 0 1 0	$2(V_i/16)$
0 0 1 1	$3(V_i/16)$
0 1 0 0	$4(V_i/16)$
0 1 0 1	$5(V_i/16)$
0 1 1 0	$6(V_i/16)$
0 1 1 1	$7(V_i/16)$
1 0 0 0	$8(V_i/16)$
1 0 0 1	$9(V_i/16)$
1 0 1 0	$10(V_i/16)$
1 0 1 1	$11(V_i/16)$
1 1 0 0	$12(V_i/16)$
1 1 0 1	$13(V_i/16)$
1 1 1 0	$14(V_i/16)$
1 1 0 1	$15(V_i/16)$

Summary:

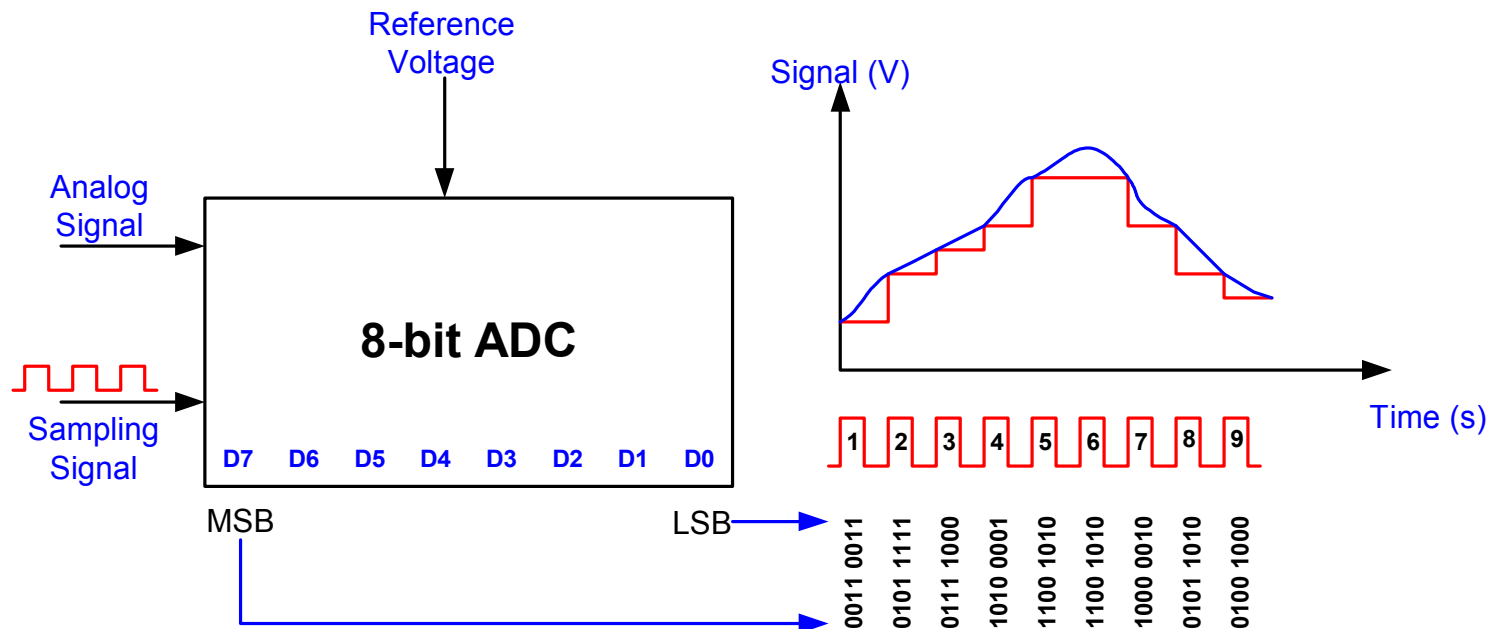
$$V_{\text{ref}} = k \times 2^N$$

$$V_{\text{full scale}} = k \times (2^N - 1)$$

Full scale

Analog to Digital Converter (A/D)

The analog to digital converter (A/D) is a device that receives as its input the analog signal along with instructions regarding the sampling rate and scaling parameters corresponding to the desired resolution of the system. The output of the A/D is a binary number at each sampling time.



Analog to Digital Converter (ADC)



Resolution

The resolution of A/D converter is defined in terms of the smallest voltage increment that will cause a bit change (LSB).

$$\text{Resolution} = \frac{\text{Reference voltage}}{2^N}$$

N – the number of the output bit

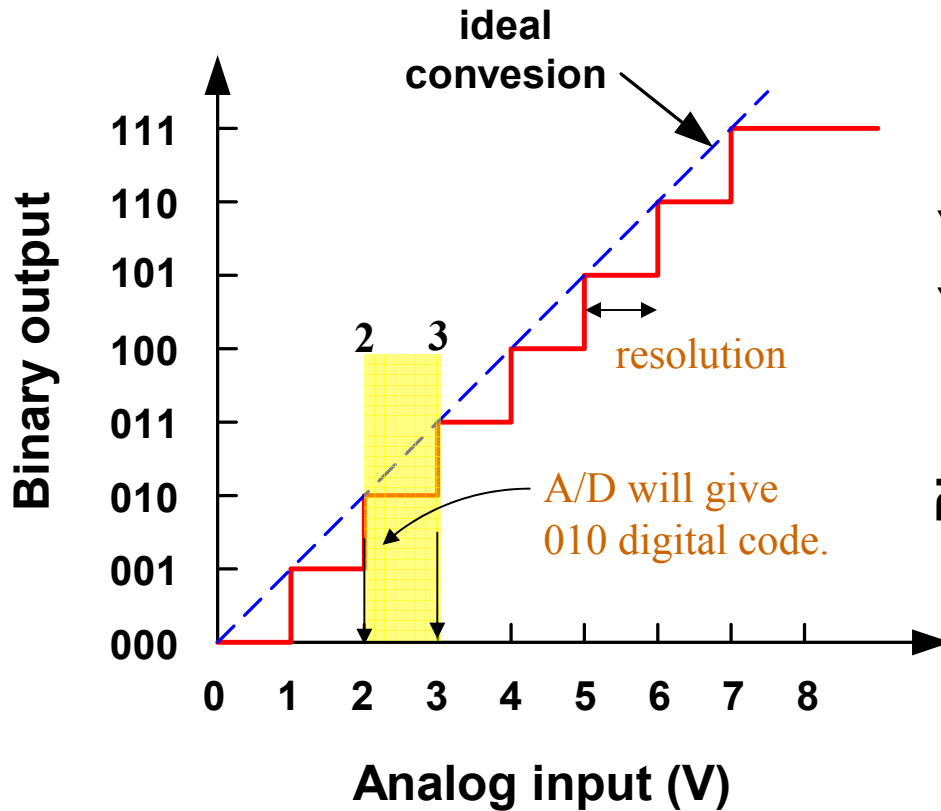
Quantization error

The limited resolution of A/D converter brings about the possibility of an error between the actual input analog value and the binary value assigned by the A/D converter

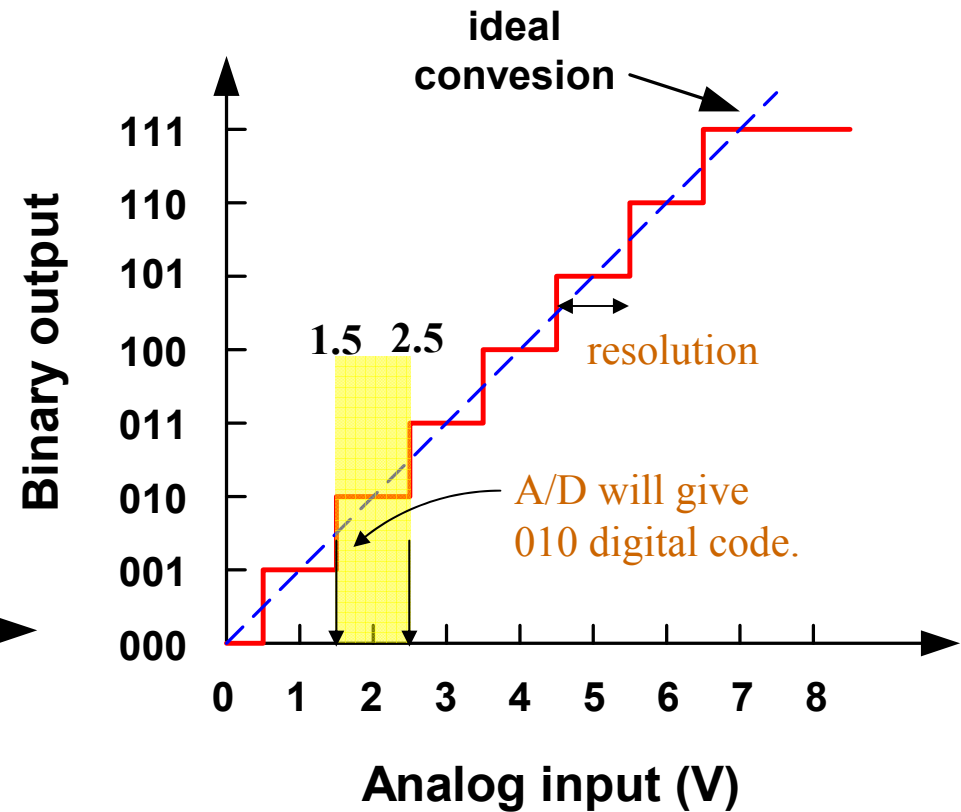
Conversion error

The total error can be calculated from all elementary errors occurring during the conversion, e.g. hysteresis, linearity, sensitivity etc.

Analog to Digital Converter (ADC)



Absolute Quantization error = 1 resolution



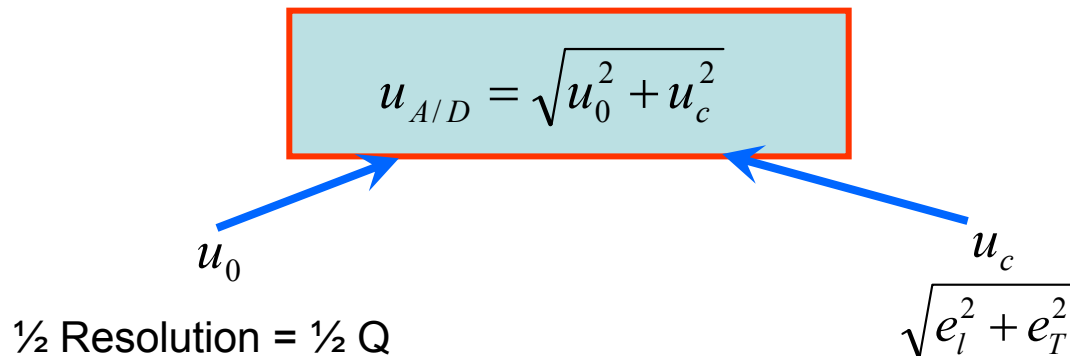
Absolute Quantization error = $\pm 1/2$ resolution

Analog to Digital Converter (ADC)

Example: The A/D converter with the following specifications listed to be used in an environment in which the A/D converter temperature may change by $\pm 10^\circ\text{C}$. Estimate the contribution of conversion and quantization errors to the uncertainty in the digital representation of an analog voltage by the converter.

	A/D converter
Reference voltage	0 – 10 V
The number of bits	12 bits
Linearity	± 3 bits
Temperature drift	1 bit/ 5°C

Solution:


$$u_{A/D} = \sqrt{u_0^2 + u_c^2}$$

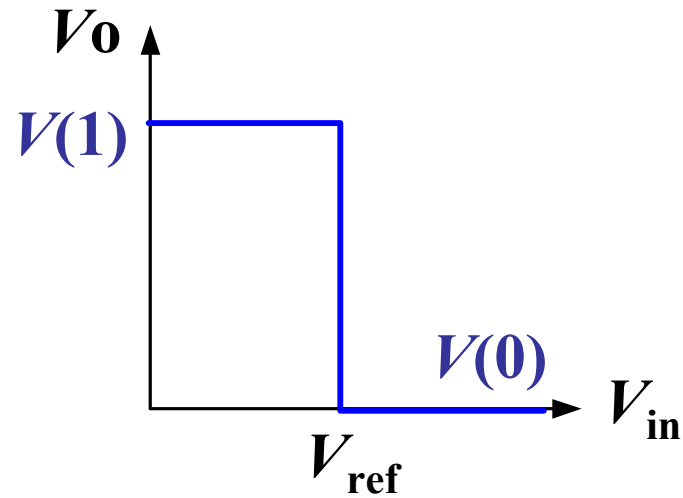
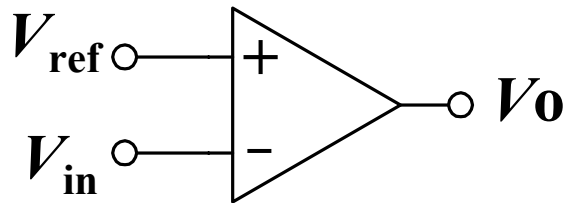
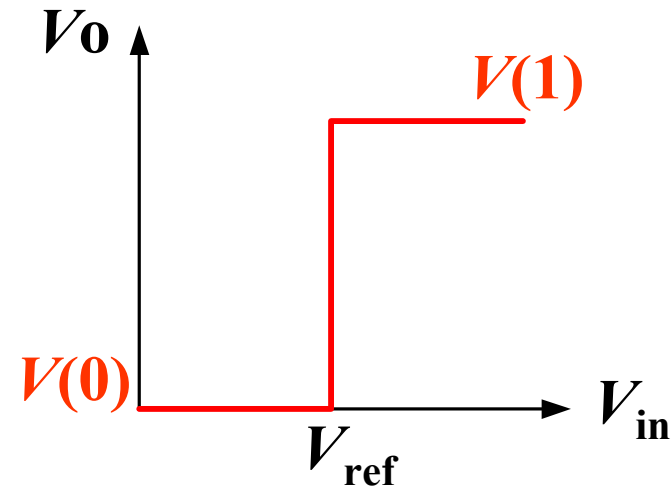
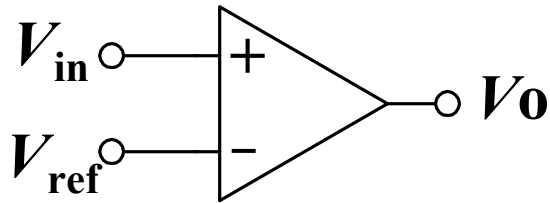
u_0
 $\frac{1}{2}$ Resolution = $\frac{1}{2}$ Q

u_c
 $\sqrt{e_l^2 + e_T^2}$

Comparator

$V_+ > V_-$; $V_o = V(1)$ Logic high

$V_+ < V_-$; $V_o = V(0)$ Logic low



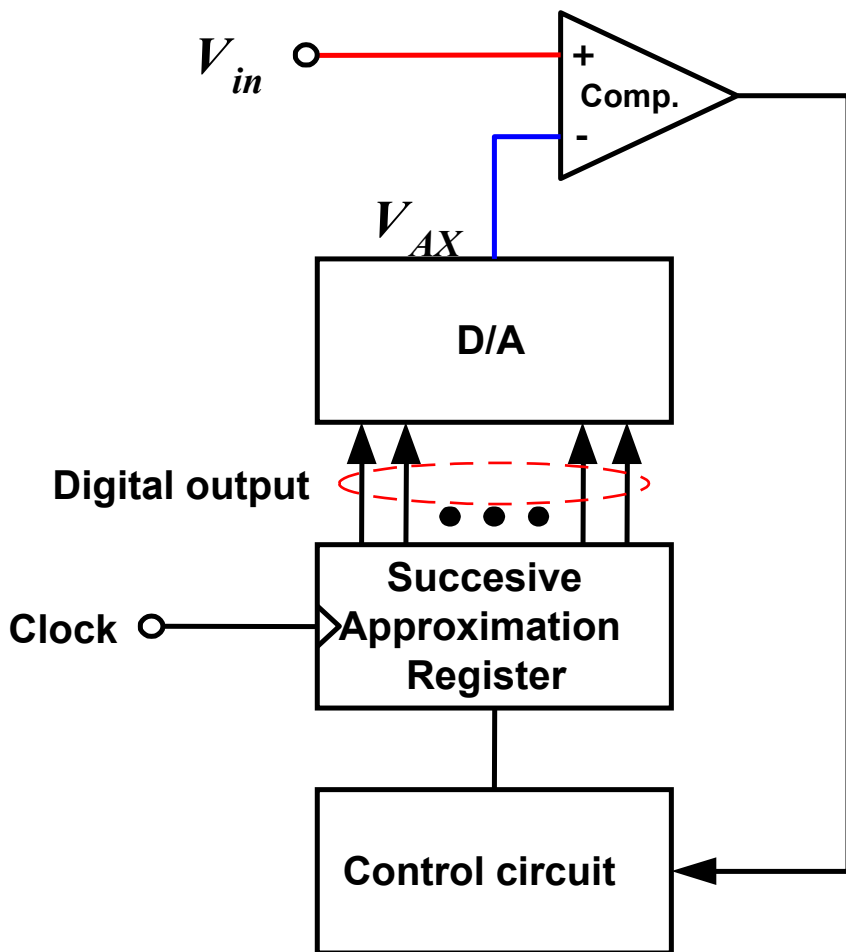
Successive Approximation A/D

Ex. To determine a number between 0 – 511 (9 bit binary),
given, the number to be determined is 301

No.	Estimate		Results
1	256	1 0000 0000	$V_{in} > V_{AX}$
2	256+128 = 384	1 1 000 0000	<
3	256+64 = 320	1 0 1 00 0000	<
4	256+32 = 288	1 00 1 0 0000	>
5	288+16 = 304	1 00 1 1 0000	<
6	288+8 = 296	1 00 1 0 1 000	>
7	296+4 = 300	1 00 1 0 1 1 00	>
8	300+2 = 302	1 00 1 0 1 1 1 0	<
9	300+1 = 301	1 00 1 0 1 1 1 1	Finished

Successive Approximation A/D

Compare the input voltage to the internally generated voltage

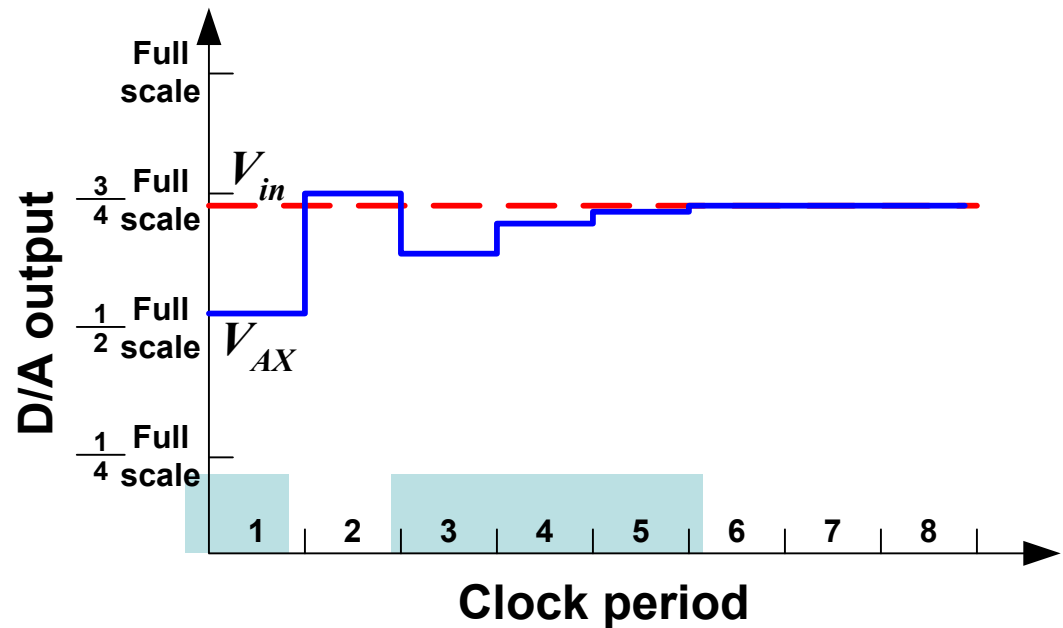


Block diagram

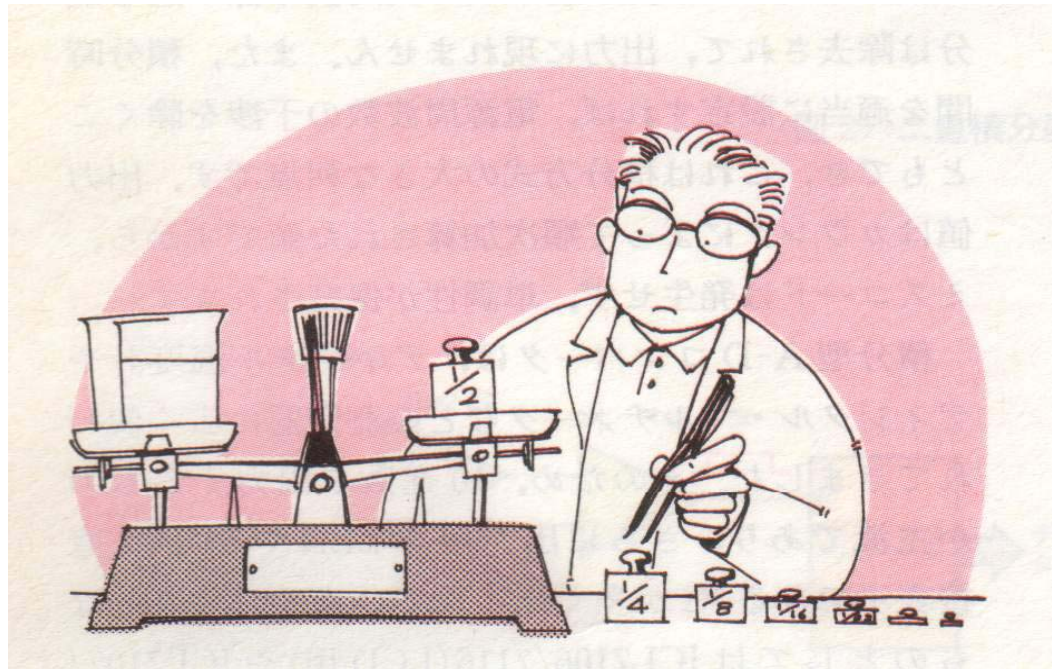
- The most common A/D for general applications
- Conversion time is fixed (not depend on the signal magnitude) and relatively fast

$$T_C = N \times \text{Clock period}$$

where N is the number of bits

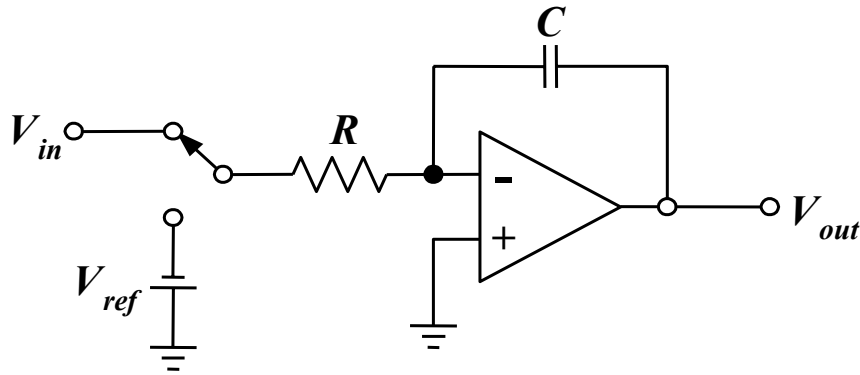


Successive Approximation A/D



Successive approximation method

Dual Slope A/D

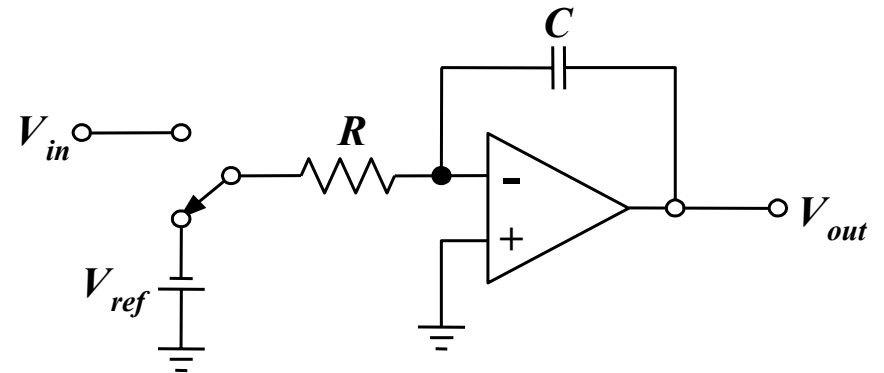
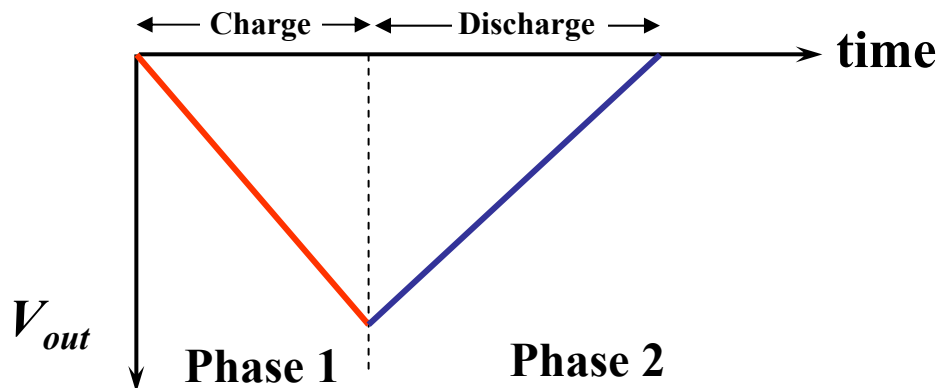


Phase 1: charging C with the unknown input for a given time.

Assume $V_c(0) = 0$

$$V_{out1} = -\frac{V_{in} T}{RC}$$

where T is the charging time



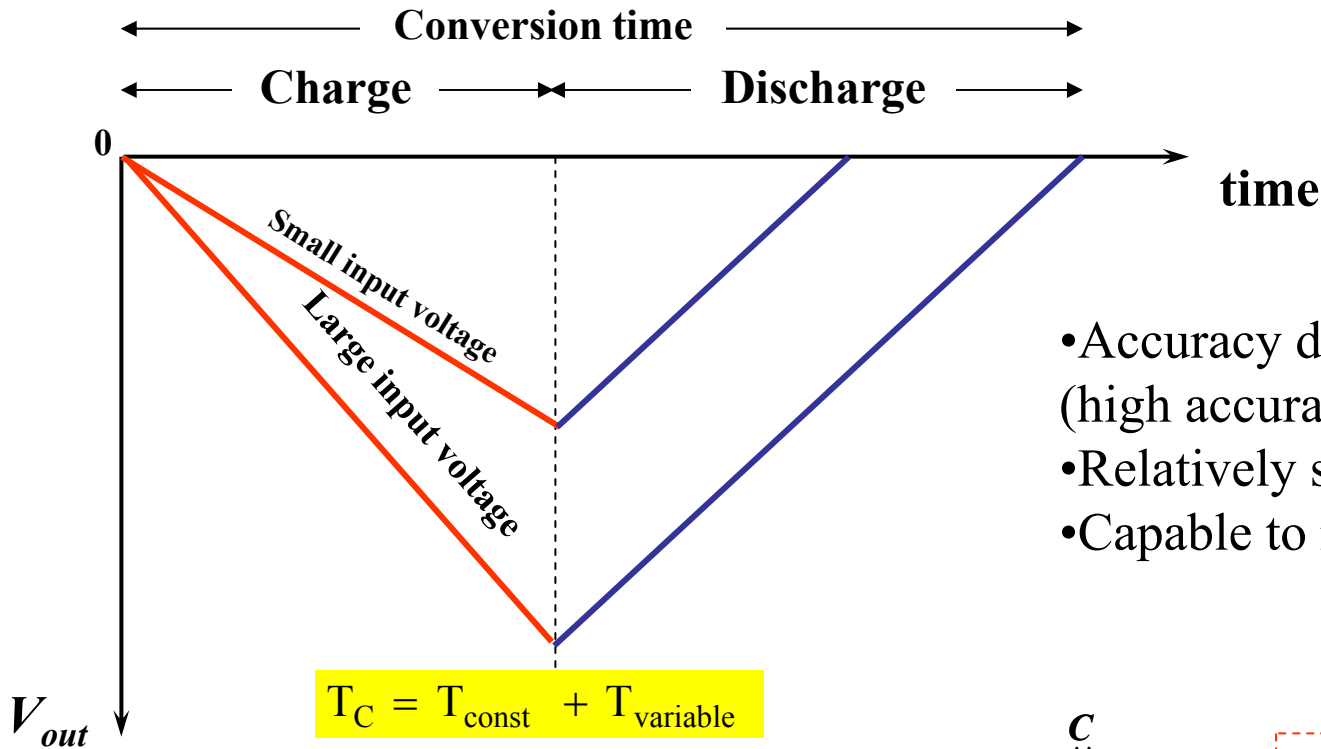
Phase 2: discharging C with the reference voltage until the output voltage goes to zero.

$$V_{out} = \frac{V_{ref} T_x}{RC} + V_{out1}$$

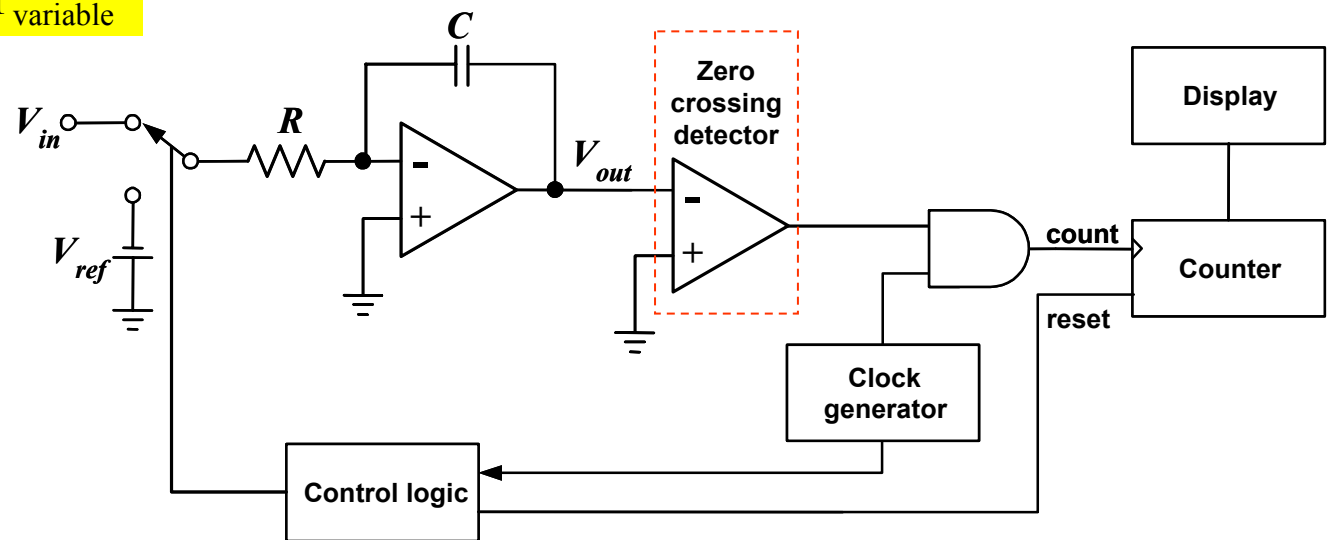
find T_x at which V_{out} becomes zero

$$T_x = \frac{V_{in} T}{V_{ref}}$$

Dual-slope Digital Voltmeter



- Accuracy does not depend on $R C$ and Clock (high accuracy)
- Relatively slow
- Capable to reject noise



Ex A dual slope A/D has $R = 100 \text{ k}\Omega$ and $C = 0.01 \text{ }\mu\text{F}$. The reference voltage is 10 volts and the fixed integration time is 10 ms. Find the conversion time for a 6.8 volt input.

$$T_x = \frac{V_{in} T}{V_{ref}} = \frac{(6.8 \text{ V})(10 \text{ ms})}{(10 \text{ V})} = 6.8 \text{ ms}$$

The total conversion time is then $10 \text{ ms} + 6.8 \text{ ms} = 16.8 \text{ ms}$

Ans

Ex Find the successive approximation A/D output for a 4-bit converter to a 3.217 volt input if the reference is 5 volts.

- (1) Set $D_3 = 1$ $V_{AX} = 5/2 = 2.5 \text{ Volts}$
 $V_{in} > V_{AX}$ leave $D_3 = 1$
- (2) Set $D_2 = 1$ $V_{AX} = 5/2 + 5/4 = 3.75 \text{ Volts}$
 $V_{in} < V_{AX}$ reset $D_2 = 0$
- (3) Set $D_1 = 1$ $V_{AX} = 5/2 + 5/8 = 3.125 \text{ Volts}$
 $V_{in} > V_{AX}$ leave $D_1 = 1$
- (4) Set $D_0 = 1$ $V_{AX} = 5/2 + 5/8 + 5/16 = 3.4375 \text{ Volts}$
 $V_{in} < V_{AX}$ reset $D_0 = 0$

By this procedure, we find the output is a binary word of 1010_2

Ans